

Heavy Photon Search DAQ and Trigger – test run

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Requirements

- 50kHz event rate at Event Builder
- 250MB/s data rate at Event Builder (calorimeter 25MB/s, muon 6MB/s, SVT 215MB/s) <40MB/s
- 100MB/s data rate on tape (after level3 trigger) <40MB/s

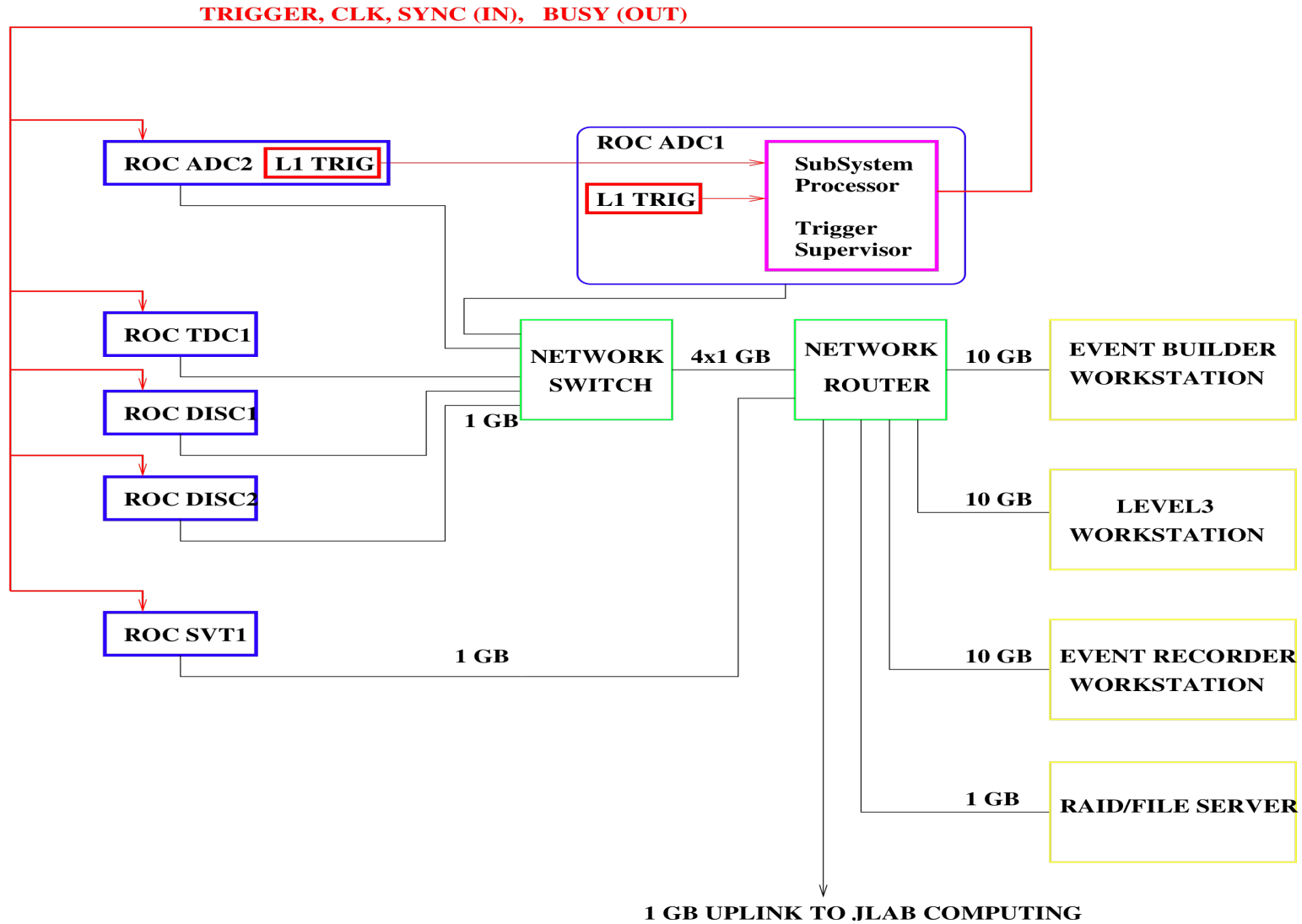
FADCs, No New Trigger

<50kHz event rate at Event Builder

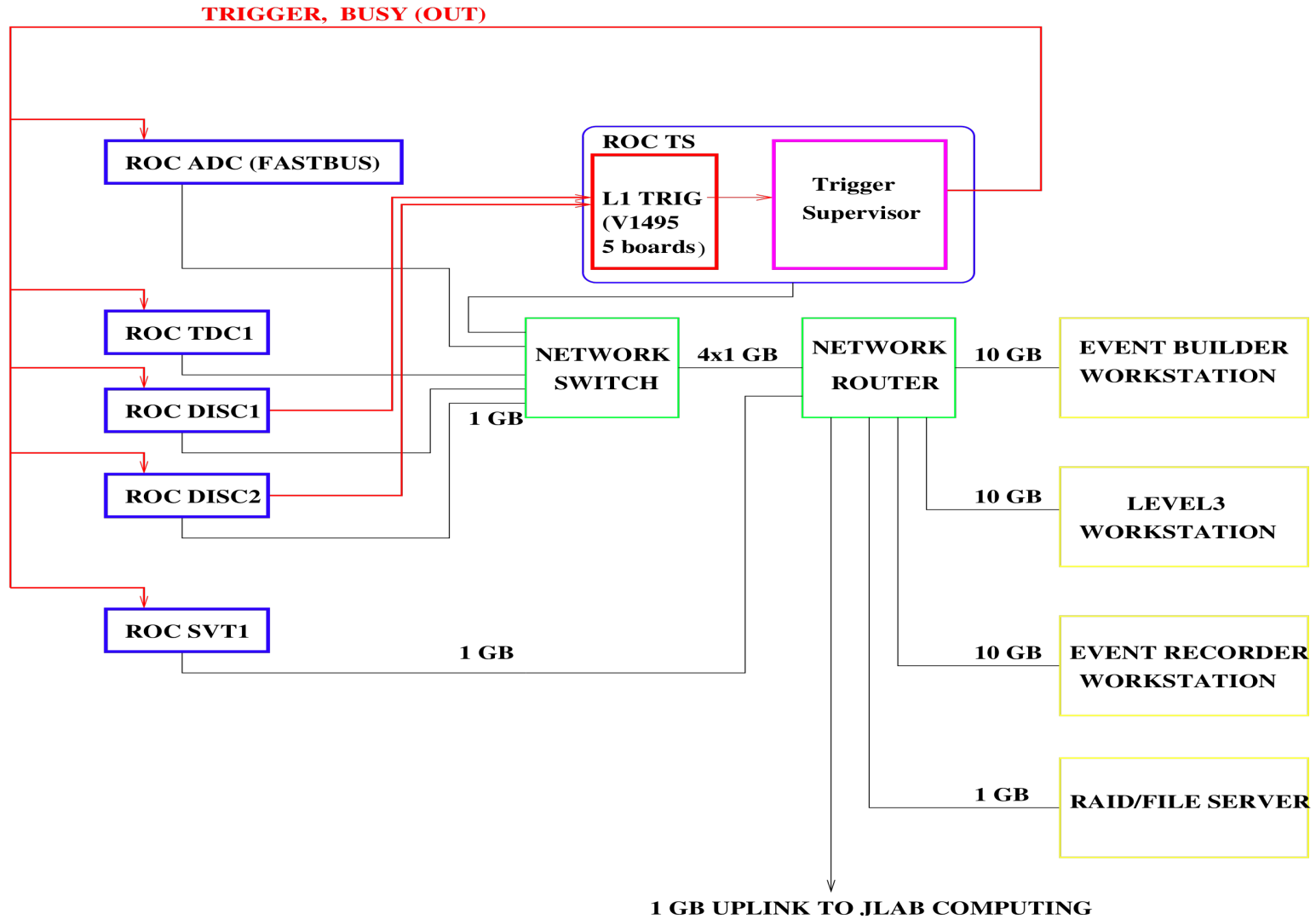
No FADCs

<10kHz event rate at Event Builder

DAQ System Overview



DAQ System Overview



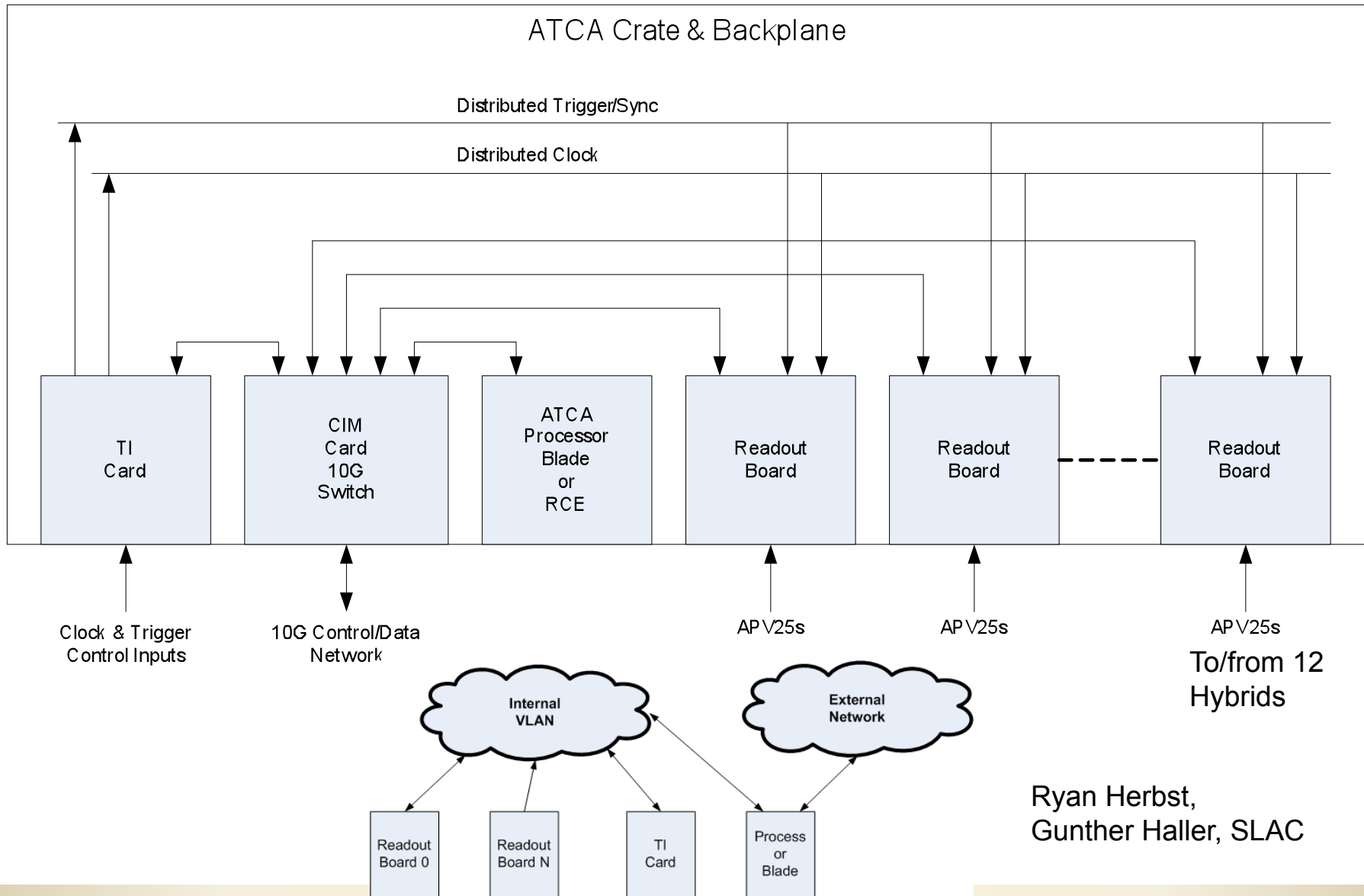
DAQ System Overview (cont.)

- SVT readout system: ?(10) boards in ATCA format
- Calorimeter and Muon System Readout: 440(704) channels of 12bit 250MHz Flash ADCs, 144 channels of 85ps resolution pipeline TDCs with discriminators
- Flash ADC - based trigger system
- 2 VME, 1 VME64X, 2(not 3) VXS, 1 ATCA crates equipped with Readout Controllers and Trigger Units
- JLAB CODA DAQ software

FADCs, no new trigger: CAEN v1495 hit-based trigger

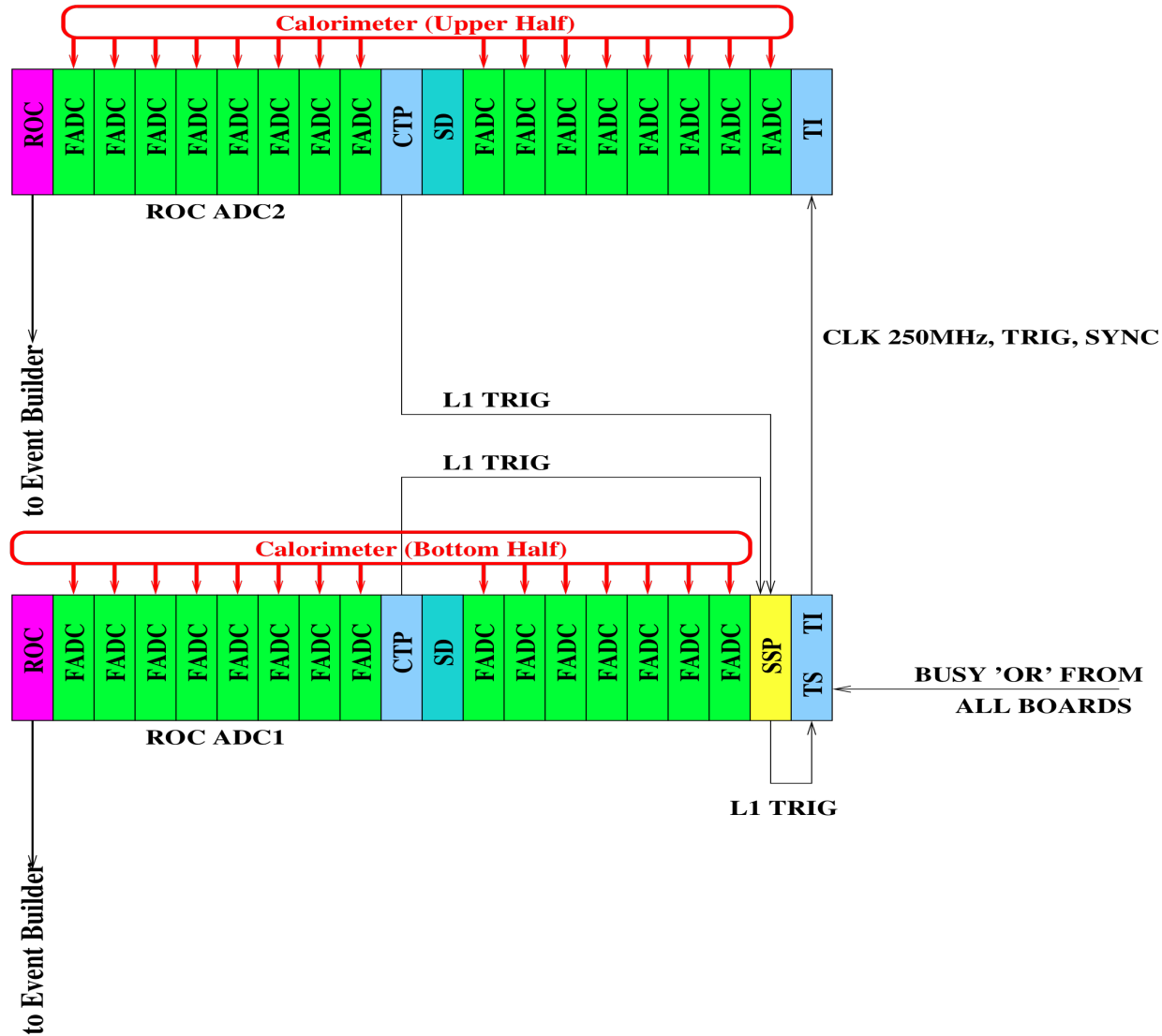
No FADCs: FASTBUS 1881M ADCs, CAEN v1495 hit-based trigger

ATCA SVT Readout System (SLAC)

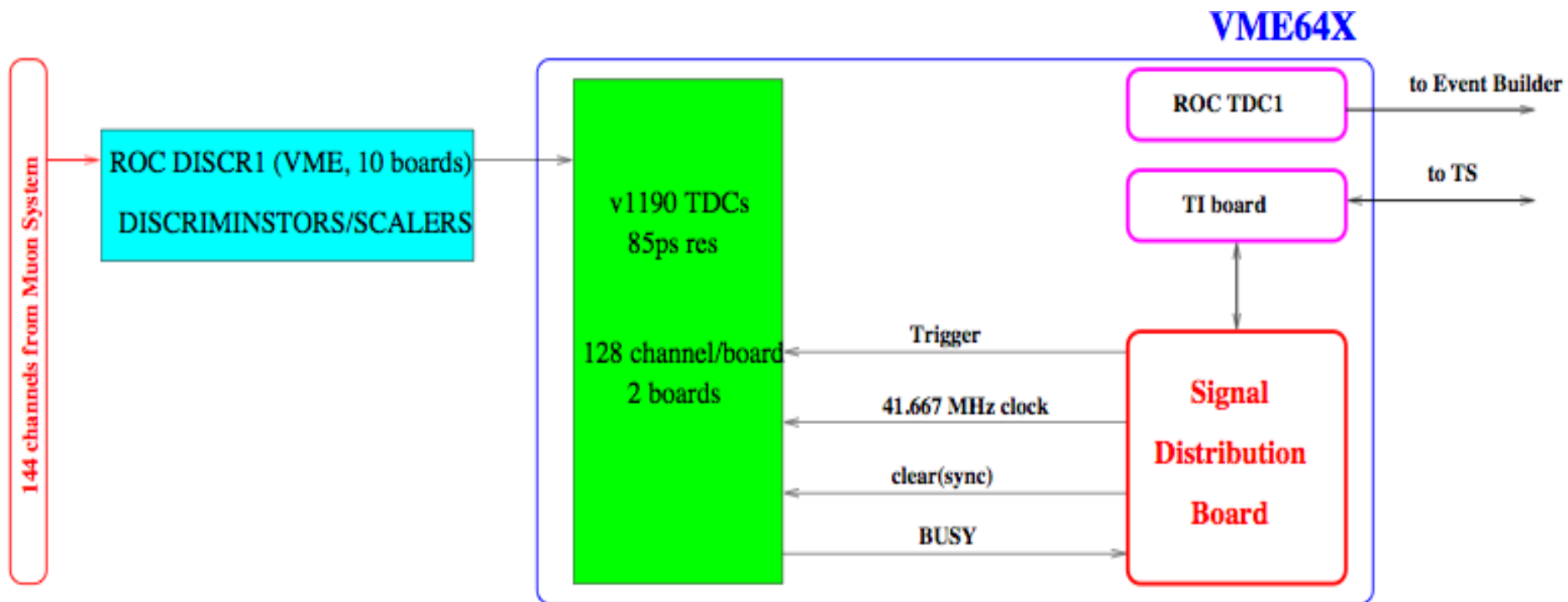


Ryan Herbst,
Gunther Haller, SLAC

Flash ADC and Trigger System (VXS)

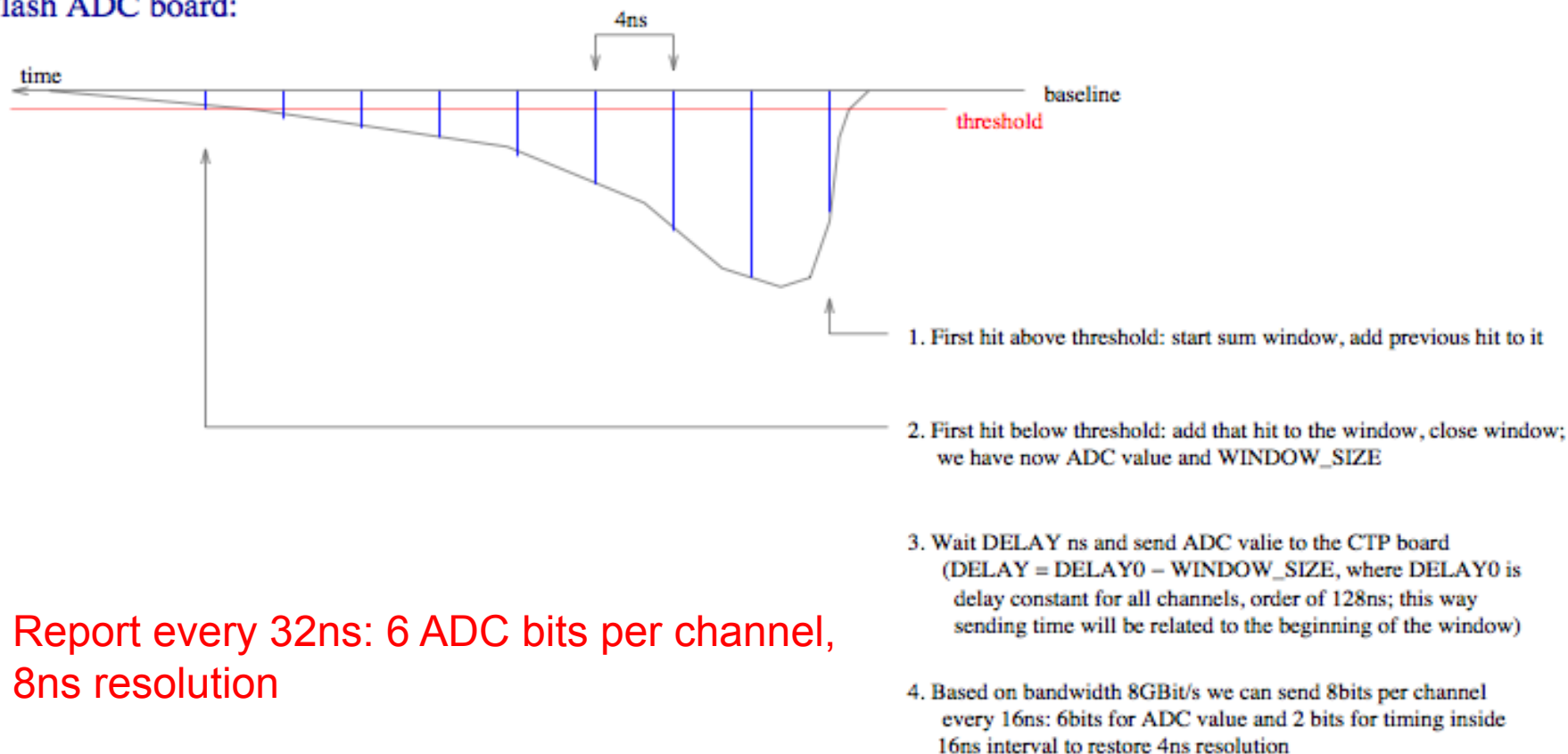


Pipeline TDC System (VME64X/VME)



Trigger processing - FADC (cont.)

Flash ADC board:



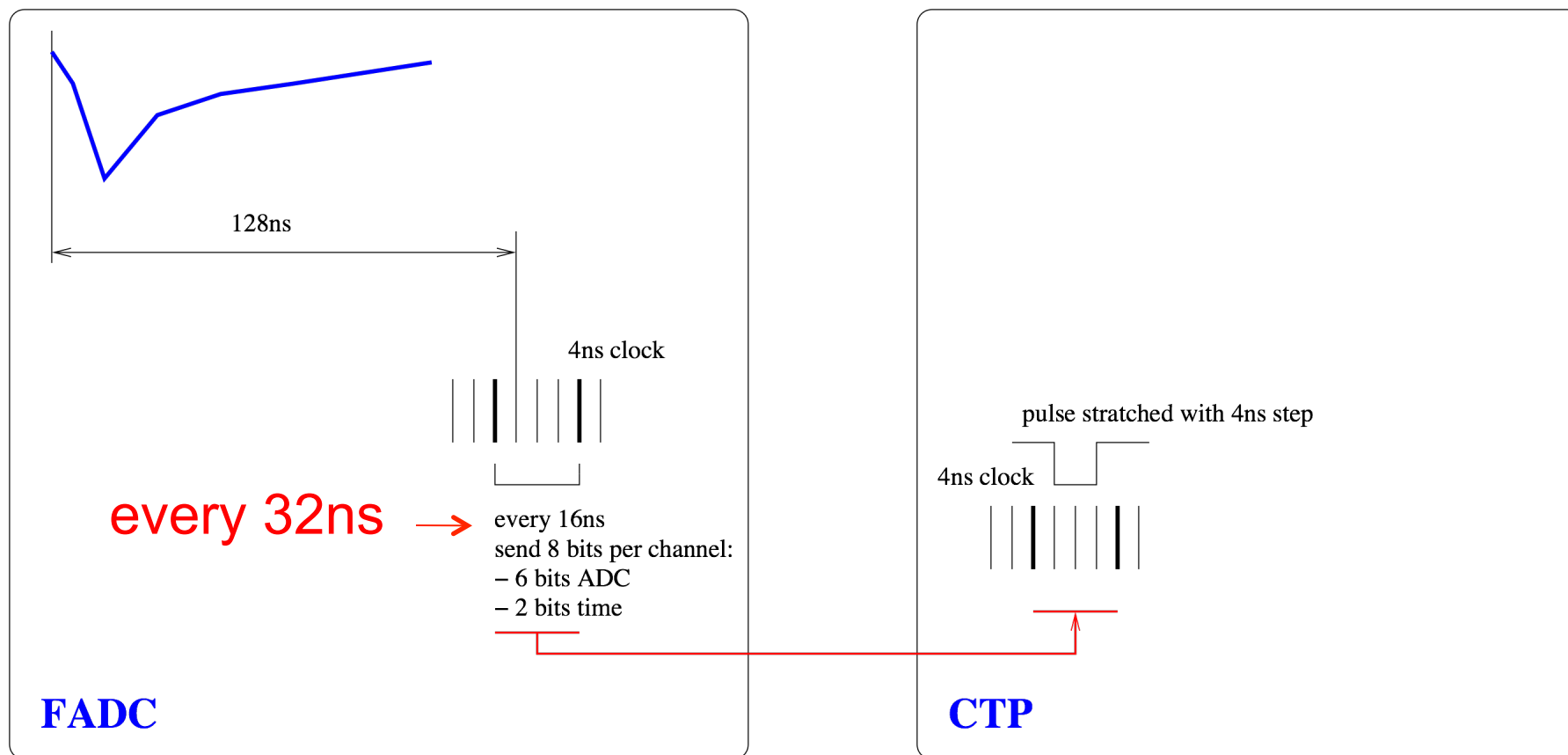
Report every 32ns: 6 ADC bits per channel,
8ns resolution

CTP board:

1. Does not have information about original sum window width
2. 4ns resolution after restoring original timing
3. Expands every window up to the value (programmable) big enough to enforce coincidence between different channels, 4ns min with 4ns step
4. Every channel has programmable delay (4ns step) and readable scaler

Flash ADC board signal processing logic

Trigger processing – FADC/CTP



Trigger processing - CTP/SSP

- Calorimeter: search for clusters using 3x3 crystals window
- Muon system: search for hits – **NOT IN TEST RUN**
- Trigger 1: two calorimeter clusters, cuts on geometry (with respect to beam) and energy (two thresholds)
- Trigger 2: two muon hits, cuts on geometry (upper and bottom) and energy (threshold) – **NOT IN TEST RUN**
- Possible problem: boundary effects because of segmented calorimeter readout and limited bandwidth between CTP and SSP

BIG PROJECT: WHEN WE Will DO IT ???

Timeline

- Available boards: all TDCs, VME/VME64X crates - **HAVE**
- Ordered by Nov 2010: 16 JLAB-made discriminator/scaler boards - **HAVE**
- Ordered by Jan 2011: 16 FADCs, 3 CTPs, 3 SDs, 3 TIs, 3 Signal Distribution Boards - **HAVE Signal Distribution Boards**
- Not ordered but needed: 32 FADC boards, 1 SSP board, VXS crates, crate controllers – **HAVE VXS crates, crate controllers**
- Oct 2010 - Jan 2011: FADC, CTP and SSP trigger FPGAs programming
- Feb 2011: testing starts with partially assembled system (without SVT readout)
- Feb 2011: SVT Board available
- April 2011: testing continues with SVT readout
- Jun 2011: complete DAQ/trigger system (without final SVT which is available in Fall)

PLAN

1. Will not use CAEN FADCs – no money
2. Reassemble and check old hit-based trigger – start now, needed anyway
3. If no FDCs on August 31 – go with FASTBUS